Abstract

A computer system includes a host processor and a peripheral device coupled by an attachment bus. The peripheral device transfers data to the host processor over the attachment bus using at least two types of data transfers. The peripheral device includes a classifying circuit that separates the data into a first class associated with a first type of transfer and a second class associated with a second type of transfer. The peripheral circuit also includes two queues, including a first queue that receives the first class of data from the classifying circuit and a second queue that receives the second class of data from the classifying circuit. A control circuit places data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus.